Amendments to the Claims

1. (PREVIOUSLY PRESENTED) A thin film Silicon on Insulator (SOI) device comprising a source, a gate, a drain, an SOI layer, and a substrate layer, the substrate layer being maintained at a potential enough lower than the source so that a parasitic MOS channel is formed between the source and drain; and a Deep N implant layer formed between either the source or drain and the parasitic MOS channel to prevent the flow of current between the source and drain via the parasitic MOS channel when the device is in an off state.

2. (PREVIOUSLY PRESENTED) The device of claim 1 wherein the Deep N implant layer is formed between the source and the parasitic MOS channel.

3. (PREVIOUSLY PRESENTED) The device of claim 1 wherein the Deep N implant layer is formed between the drain and the parasitic MOS channel.

Claims 4-6 (*Cancelled*)

Claims 7-11 (*Cancelled*)